REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-41 are pending. Claims 1-41 have been rejected.

Claims 1, 12, 23, 25, and 26 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are rejected under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent No. 6,282,556 to Chehrazi (hereinafter "Chehrazi") in view of U.S. Patent No. 6,036,350 to Mennemeier ("Mennemeier").

Applicants respectfully submit that claim 1, as amended, is not obvious under 35 U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

Amended claim 1 includes receiving a first vector of numbers and a second vector of numbers; selecting a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector according to a configuration specified by the instruction; and generating **simultaneously** a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers.

It is respectfully submitted that neither Chehrazi, nor Mennemeier discloses such limitations of amended claim 1.

It is respectfully submitted that Chehrazi does not teach or suggest a combination with Mennemeier, and Mennemeier does not teach or suggest a combination with Chehrazi. It would be impermissible hindsight, based on applicants' own disclosure, to combine Chehrazi and Mennemeier.

Chehrazi discloses a pipelined data path for a media processor. More specifically, Chehrazi discloses operation of the sum of absolute difference (SABD) instruction (**Figure 20B**). Chehrazi discloses

> As shown in **FIG. 20B**, each separate operand of register 310 has a corresponding operand of register 312, e.g., operand 310(f) corresponds to operand 312(f), etc. The data path circuit 300 first uses one of its 16 8-bit subtractor circuits, 322 or 324 (**FIG. 4**), to perform subtraction on each corresponding operand pair, specifically subtracting Vs from Vt. The other 16 8-bit subtractor circuit then performs the same subtraction in parallel but between Vt from Vs. <u>This simultaneously products 32 separate differences and a positive and a negative difference for each corresponding operand pair</u>. Multiplexers in circuit 332 then select the positive difference for each operand pair as the absolute value difference for each pair. These absolute value differences are them summed together at 575 of **FIG. 20B** to arrive at a single result sum stored in register 415.

(Chehrazi, col.20, line 65-col. 21, line 12)(emphasis added)

Thus, Chehrazi merely discloses producing simultaneously 32 separate differences and <u>a positive</u> and <u>a negative</u> difference for each corresponding operand pair. In contrast, amended claim 1 refers to generating <u>simultaneously</u> a third plurality of numbers, each of which is <u>an absolute</u> difference between a number in the first plurality of numbers and a number in the second plurality of numbers.

Mennemeier, in contrast, discloses sorting signed numbers and solving absolute differences using packed instructions. More specifically, Mennemeier discloses that the absolute difference is determined by subtracting the minima from its corresponding maxima (**Figure 3B**, col. 7, line 64-col. 8, line 12).

Furthermore, even if the method of sorting signed numbers of Mennemeier were incorporated into the pipelined data path of Chehrazi, such a combination would still lack generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, as recited in amended claim 1.

Given that claims 2-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 2-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are not obvious under 35 U.S.C. § 103(a) over Chehrazi in view of Mennemeier.

The Examiner rejected claims 4, 15, 29, and 39 under 35 U.S.C. § 103(a) as being unpatentable over Chehrazi in view of Mennemeier, and further in view of European Patent No. EPO 0485776 A2 to Diefendorff et al. ("Diefendorff").

It is respectfully submitted that neither Chehrazi, Mennemeier, nor Diefendorff disclose generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, as recited in amended claim 1.

It is respectfully submitted none of the references cited by the Examiner teach or suggest a combination with each other. It would be impermissible hindsight, based on Applicants' own disclosure, to combine Chehrazi, Mennemeier, and Diefendorff.

Chehrazi discloses a pipelined data path for a media processor. Chehrazi merely discloses producing simultaneously 32 separate differences and a positive and a negative difference for each corresponding operand pair (col.20, line 65-col. 21, line 12). In contrast, amended claim 1 refers to generating simultaneously a third plurality of

numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers.

Mennemeier, in contrast, discloses sorting signed numbers and solving absolute differences using packed instructions. More specifically, Mennemeier discloses that the absolute difference is determined by subtracting the minima from its corresponding maxima (**Figure 3B**, col. 7, line 64-col. 8, line 12).

Diefendorff, in contrast, discloses a method for executing graphics pixel packing instructions (Abstract).

Furthermore, even if the method of sorting signed numbers of Mennemeier and the method of executing the pixel packing instructions of Diefendorff were incorporated into the pipelined data path of Chehrazi, such a combination would still lack generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, as recited in amended claim 1.

Given that claims 4, 15, 29, and 39 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 4, 15, 29, and 39 are not obvious under 35 U.S.C. § 103(a) over Chehrazi in view of Mennemeier, and further in view of Diefendorff.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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